

FEATURES

- Guaranteed maximum frequency >4GHz
- 3.3V and 5V power supply options
- Guaranteed propagation delay <460ps over temperature
- Internal 75kΩ input pull-down resistors
- Wide operating temperature range: -40°C to +85°C
- Available in 8-pin MSOP and SOIC packages



ECL Pro™

DESCRIPTION

The SY10/100EP33V is an integrated ÷4 divider.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC-coupled inputs. When used, decouple V_{BB} to V_{CC} via a 0.01μF capacitor and limit current sourcing or sinking to 0.5mA. When not used, V_{BB} should be left open.

The reset pin is asynchronous and is asserted on the rising edge. Upon power-up, the internal flip-flops will attain a random state; the reset allows for the synchronous use of multiple EP33s in a system.

The 100K Series includes internal temperature compensation circuitry.

PIN NAMES

| Pin | Function |
|-----------|--|
| CLK, /CLK | ECL Clock Inputs with Internal 75kΩ Pull-Down Resistor, Default State is LOW |
| RESET | ECL Asynchronous Reset |
| V_{BB} | Reference Voltage Output |
| Q, /Q | ECL Data Outputs |

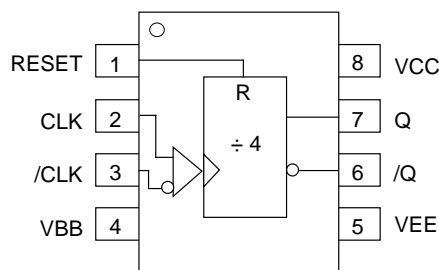
TRUTH TABLE⁽¹⁾

| CLK | /CLK | RESET | Q | /Q |
|-----|------|------------------|---|----|
| X | X | Z ⁽²⁾ | L | H |
| ┌ | └ | L | F | F |

Notes:

1. F = Divide by 4 function.
2. Z = Low to High transition.

PACKAGE/ORDERING INFORMATION



TOP VIEW
(Available in MSOP or SOIC package)

Ordering Information⁽¹⁾

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|----------------------------------|--------------|-----------------|--|----------------|
| SY10EP33VZC | Z8-1 | Commercial | HEP33V | Sn-Pb |
| SY10EP33VZCTR ⁽²⁾ | Z8-1 | Commercial | HEP33V | Sn-Pb |
| SY100EP33VZC | Z8-1 | Commercial | XEP33V | Sn-Pb |
| SY100EP33VZCTR ⁽²⁾ | Z8-1 | Commercial | XEP33V | Sn-Pb |
| SY10EP33VKC | K8-1 | Commercial | HP33 | Sn-Pb |
| SY10EP33VKCTR ⁽²⁾ | K8-1 | Commercial | HP33 | Sn-Pb |
| SY100EP33VKC | K8-1 | Commercial | XP33 | Sn-Pb |
| SY100EP33VKCTR ⁽²⁾ | K8-1 | Commercial | XP33 | Sn-Pb |
| SY10EP33VZI | Z8-1 | Industrial | HEP33V | Sn-Pb |
| SY10EP33VZITR ⁽²⁾ | Z8-1 | Industrial | HEP33V | Sn-Pb |
| SY100EP33VZI | Z8-1 | Industrial | XEP33V | Sn-Pb |
| SY100EP33VZITR ⁽²⁾ | Z8-1 | Industrial | XEP33V | Sn-Pb |
| SY10EP33VKI | K8-1 | Industrial | HP33 | Sn-Pb |
| SY10EP33VKITR ⁽²⁾ | K8-1 | Industrial | HP33 | Sn-Pb |
| SY100EP33VKI | K8-1 | Industrial | XP33 | Sn-Pb |
| SY100EP33VKITR ⁽²⁾ | K8-1 | Industrial | XP33 | Sn-Pb |
| SY10EP33VZG ⁽³⁾ | Z8-1 | Industrial | HEP33V with Pb-Free bar-line indicator | NiPdAu Pb-Free |
| SY10EP33VZGTR ^(2, 3) | Z8-1 | Industrial | HEP33V with Pb-Free bar-line indicator | NiPdAu Pb-Free |
| SY100EP33VZG ⁽³⁾ | Z8-1 | Industrial | XEP33V with Pb-Free bar-line indicator | NiPdAu Pb-Free |
| SY100EP33VZGTR ^(2, 3) | Z8-1 | Industrial | XEP33V with Pb-Free bar-line indicator | NiPdAu Pb-Free |
| SY10EP33VKG ⁽³⁾ | K8-1 | Industrial | HP33 with Pb-Free bar-line indicator | NiPdAu Pb-Free |
| SY10EP33VKGTR ^(2, 3) | K8-1 | Industrial | HP33 with Pb-Free bar-line indicator | NiPdAu Pb-Free |
| SY100EP33VKG ⁽³⁾ | K8-1 | Industrial | XP33 with Pb-Free bar-line indicator | NiPdAu Pb-Free |
| SY100EP33VKGTR ^(2, 3) | K8-1 | Industrial | XP33 with Pb-Free bar-line indicator | NiPdAu Pb-Free |

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Rating | Value | Unit | |
|--------------------|--|------------------------|--------|------|
| V _{CC} | Power Supply Voltage (V _{EE} = 0) | +6.0 to 0 | V | |
| V _{EE} | Power Supply Voltage (V _{CC} = 0) | -6.0 to 0 | V | |
| V _{IN} | Input Voltage (V _{CC} = 0V, V _{IN} not more negative than V _{EE}) Input Voltage (V _{EE} = 0V, V _{IN} not more positive than V _{CC}) | -6.0 to 0 +6.0 to 0 | V V | |
| I _{OUT} | Output Current -Continuous -Surge | 50 100 | mA | |
| T _A | Operating Temperature Range | -40 to +85 | °C | |
| T _{LEAD} | Lead Temperature | +260 | °C | |
| T _{store} | Storage Temperature Range | -65 to +150 | °C | |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) SOIC-8 | -Still Air | 160 | °C/W |
| | | -500lfpm | 109 | °C/W |
| | MSOP-8 | -Still Air | 206 | °C/W |
| | | -500lfpm | 155 | °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) | SOIC-8 | 39 | °C/W |
| | | MSOP-8 | 39 | °C/W |

Note:
1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(10EP) LVPECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾

V_{CC} = +3.3V ±10%; V_{EE} = 0V⁽²⁾

| Symbol | Parameter | T _A = -40°C | | | T _A = +25°C | | | T _A = +85°C | | | Unit |
|--------------------|---|------------------------|--------|-----------------|------------------------|--------|-----------------|------------------------|--------|-----------------|------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| I _{EE} | Power Supply Current | — | — | 36 | — | 26 | 36 | — | — | 36 | mA |
| V _{OH} | Output HIGH Voltage ⁽³⁾ | 2165 | 2290 | 2415 | 2230 | 2355 | 2480 | 2290 | 2415 | 2540 | mV |
| V _{OL} | Output LOW Voltage ⁽³⁾ | 1365 | 1490 | 1615 | 1430 | 1555 | 1680 | 1490 | 1615 | 1740 | mV |
| V _{IH} | Input HIGH Voltage (Single-Ended) | 2090 | — | 2415 | 2155 | — | 2480 | 2215 | — | 2540 | mV |
| V _{IL} | Input LOW Voltage (Single-Ended) | 1365 | — | 1690 | 1430 | — | 1755 | 1490 | — | 1815 | mV |
| V _{BB} | Output Voltage | 1790 | 1890 | 1990 | 1885 | 1955 | 2055 | 1915 | 2015 | 2115 | mV |
| V _{IHCMR} | Input HIGH Voltage ⁽⁴⁾ Common Mode Range (Differential) | 2.0 | — | V _{CC} | 2.0 | — | V _{CC} | 2.0 | — | V _{CC} | V |
| I _{IH} | Input HIGH Current | — | — | 150 | — | — | 150 | — | — | 150 | µA |
| I _{IL} | Input LOW Current RESET, CLK /CLK | 0.5 -150 | — — | — — | 0.5 -150 | — — | — — | 0.5 -150 | — — | — — | µA |

Notes:
1. 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.
2. Input and output parameters vary 1:1 with V_{CC}.
3. All loading with 50Ω to V_{CC} -2.0V.
4. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

(10EP) PECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾

$V_{CC} = +5.0V \pm 10\%$; $V_{EE} = 0V^{(2)}$

| Symbol | Parameter | $T_A = -40^\circ C$ | | | $T_A = +25^\circ C$ | | | $T_A = +85^\circ C$ | | | Unit |
|-------------|--|---------------------|--------|----------|---------------------|--------|----------|---------------------|--------|----------|---------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| I_{EE} | Power Supply Current | — | — | 36 | — | 26 | 36 | — | — | 36 | mA |
| V_{OH} | Output HIGH Voltage ⁽³⁾ | 3865 | 3990 | 4115 | 3930 | 4055 | 4180 | 3990 | 4115 | 4240 | mV |
| V_{OL} | Output LOW Voltage ⁽³⁾ | 3065 | 3190 | 3315 | 3130 | 3255 | 3380 | 3190 | 3315 | 3440 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 3790 | — | 4115 | 3855 | — | 4180 | 3915 | — | 4240 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 3065 | — | 3390 | 3130 | — | 3455 | 3190 | — | 3515 | mV |
| V_{BB} | Output Voltage | 3490 | 3590 | 3690 | 3555 | 3655 | 3755 | 3615 | 3715 | 3815 | mV |
| V_{IHCMR} | Input HIGH Voltage ⁽⁴⁾ Common Mode Range (Differential) | 2.0 | — | V_{CC} | 2.0 | — | V_{CC} | 2.0 | — | V_{CC} | V |
| I_{IH} | Input HIGH Current | — | — | 150 | — | — | 150 | — | — | 150 | μA |
| I_{IL} | Input LOW Current RESET, CLK /CLK | 0.5 -150 | — — | — — | 0.5 -150 | — — | — — | 0.5 -150 | — — | — — | μA |

Notes:

- 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.
- Input and output parameters vary 1:1 with V_{CC} .
- All loading with 50Ω to $V_{CC} - 2.0V$.
- The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

(10EP) ECL/LVECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾

$V_{CC} = 0V$; $V_{EE} = -3.3V$ to $-5.0V \pm 10\%^{(2)}$

| Symbol | Parameter | $T_A = -40^\circ C$ | | | $T_A = +25^\circ C$ | | | $T_A = +85^\circ C$ | | | Unit |
|-------------|--|---------------------|--------|--------|---------------------|--------|--------|---------------------|--------|--------|---------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| I_{EE} | Power Supply Current | — | — | 36 | — | 26 | 36 | — | — | 36 | mA |
| V_{OH} | Output HIGH Voltage ⁽³⁾ | -1135 | -1010 | -885 | -1070 | -945 | -820 | -1010 | -885 | -760 | mV |
| V_{OL} | Output LOW Voltage ⁽³⁾ | -1935 | -1810 | -1685 | -1870 | -1745 | -1620 | -1810 | -1685 | -1560 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1210 | — | -885 | -1145 | — | -820 | -1085 | — | -760 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1935 | — | -1610 | -1870 | — | -1545 | -1810 | — | -1485 | mV |
| V_{BB} | Output Voltage | -1510 | -1410 | -1310 | -1445 | -1345 | -1245 | -1385 | -1285 | -1185 | mV |
| V_{IHCMR} | Input HIGH Voltage ⁽⁴⁾ Common Mode Range (Differential) | $V_{EE} + 2.0$ | | 0.0 | $V_{EE} + 2.0$ | | 0.0 | $V_{EE} + 2.0$ | | 0.0 | V |
| I_{IH} | Input HIGH Current | — | — | 150 | — | — | 150 | — | — | 150 | μA |
| I_{IL} | Input LOW Current RESET, CLK /CLK | 0.5 -150 | — — | — — | 0.5 -150 | — — | — — | 0.5 -150 | — — | — — | μA |

Notes:

- 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.
- Input and output parameters vary 1:1 with V_{CC} .
- All loading with 50Ω to $V_{CC} - 2.0V$.
- V_{IHCMR} (Min) varies 1:1 with V_{EE} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

(100EP) LVPECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾

$V_{CC} = +3.3V \pm 10\%$; $V_{EE} = 0V^{(2)}$

| Symbol | Parameter | $T_A = -40^\circ C$ | | | $T_A = +25^\circ C$ | | | $T_A = +85^\circ C$ | | | Unit |
|-------------|--|---------------------|--------|----------|---------------------|--------|----------|---------------------|--------|----------|---------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| I_{EE} | Power Supply Current | — | — | 36 | — | 30 | 36 | — | — | 40 | mA |
| V_{OH} | Output HIGH Voltage ⁽³⁾ | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | 2155 | 2280 | 2405 | mV |
| V_{OL} | Output LOW Voltage ⁽³⁾ | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | 1355 | 1480 | 1605 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 2075 | — | 2420 | 2075 | — | 2420 | 2075 | — | 2420 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 1355 | — | 1675 | 1355 | — | 1675 | 1355 | — | 1675 | mV |
| V_{BB} | Output Voltage | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | 1775 | 1875 | 1975 | mV |
| V_{IHCMR} | Input HIGH Voltage ⁽⁴⁾ Common Mode Range (Differential) | 2.0 | — | V_{CC} | 2.0 | — | V_{CC} | 2.0 | — | V_{CC} | V |
| I_{IH} | Input HIGH Current | — | — | 150 | — | — | 150 | — | — | 150 | μA |
| I_{IL} | Input LOW Current RESET, CLK /CLK | 0.5 -150 | — — | — — | 0.5 -150 | — — | — — | 0.5 -150 | — — | — — | μA |

Notes:

- 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.
- Input and output parameters vary 1:1 with V_{CC} .
- All loading with 50Ω to $V_{CC} - 2.0V$.
- The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

(100EP) PECL DC ELECTRICAL CHARACTERISTICS⁽¹⁾

$V_{CC} = +5.0V \pm 10\%$; $V_{EE} = 0V^{(2)}$

| Symbol | Parameter | $T_A = -40^\circ C$ | | | $T_A = +25^\circ C$ | | | $T_A = +85^\circ C$ | | | Unit |
|-------------|--|---------------------|--------|----------|---------------------|--------|----------|---------------------|--------|----------|---------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| I_{EE} | Power Supply Current | — | — | 36 | — | 30 | 36 | — | — | 40 | mA |
| V_{OH} | Output HIGH Voltage ⁽³⁾ | 3855 | 3980 | 4105 | 3855 | 3980 | 4105 | 3855 | 3980 | 4105 | mV |
| V_{OL} | Output LOW Voltage ⁽³⁾ | 3055 | 3180 | 3305 | 3055 | 3180 | 3305 | 3055 | 3180 | 3305 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | 3775 | — | 4120 | 3775 | — | 4120 | 3775 | — | 4120 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | 3055 | — | 3375 | 3055 | — | 3375 | 3055 | — | 3375 | mV |
| V_{BB} | Output Voltage | 3475 | 3575 | 3675 | 3475 | 3575 | 3675 | 3475 | 3575 | 3675 | mV |
| V_{IHCMR} | Input HIGH Voltage ⁽⁴⁾ Common Mode Range (Differential) | 2.0 | — | V_{CC} | 2.0 | — | V_{CC} | 2.0 | — | V_{CC} | V |
| I_{IH} | Input HIGH Current | — | — | 150 | — | — | 150 | — | — | 150 | μA |
| I_{IL} | Input LOW Current RESET, CLK /CLK | 0.5 -150 | — — | — — | 0.5 -150 | — — | — — | 0.5 -150 | — — | — — | μA |

Notes:

- 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.
- Input and output parameters vary 1:1 with V_{CC} .
- All loading with 50Ω to $V_{CC} - 2.0V$.
- The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

(100EP) ECL/LVECL DC ELECTRICAL CHARACTERISTICS(1)

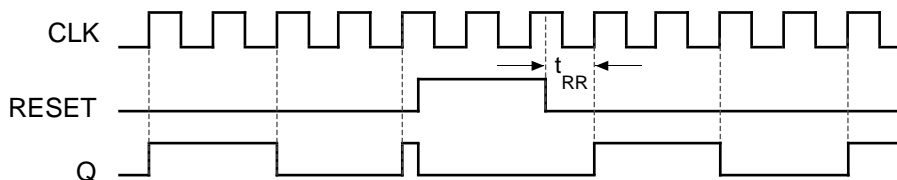
$V_{CC} = 0V$; $V_{EE} = -3.3V$ to $-5.0V \pm 10\%$ (2)

| Symbol | Parameter | $T_A = -40^\circ C$ | | | $T_A = +25^\circ C$ | | | $T_A = +85^\circ C$ | | | Unit |
|-------------|--|---------------------|--------|--------|---------------------|--------|--------|---------------------|--------|--------|---------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| I_{EE} | Power Supply Current | — | — | 36 | — | 30 | 36 | — | — | 40 | mA |
| V_{OH} | Output HIGH Voltage(3) | -1145 | -1020 | -895 | -1145 | -1020 | -895 | -1145 | -1020 | -895 | mV |
| V_{OL} | Output LOW Voltage(3) | -1945 | -1820 | -1695 | -1945 | -1820 | -1695 | -1945 | -1820 | -1695 | mV |
| V_{IH} | Input HIGH Voltage (Single-Ended) | -1225 | — | -880 | -1225 | — | -880 | -1225 | — | -880 | mV |
| V_{IL} | Input LOW Voltage (Single-Ended) | -1945 | — | -1625 | -1945 | — | -1625 | -1945 | — | -1625 | mV |
| V_{BB} | Output Voltage | -1525 | -1425 | -1325 | -1525 | -1425 | -1325 | -1525 | -1425 | -1325 | mV |
| V_{IHCMR} | Input HIGH Voltage(4) Common Mode Range (Differential) | $V_{EE} + 2.0$ | | 0.0 | $V_{EE} + 2.0$ | | 0.0 | $V_{EE} + 2.0$ | | 0.0 | V |
| I_{IH} | Input HIGH Current | — | — | 150 | — | — | 150 | — | — | 150 | μA |
| I_{IL} | Input LOW Current RESET, CLK /CLK | 0.5 -150 | — — | — — | 0.5 -150 | — — | — — | 0.5 -150 | — — | — — | μA |

Notes:

- 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and traverse airflow greater than 500lfpm is maintained.
- Input and output parameters vary 1:1 with V_{CC} .
- All loading with 50Ω to $V_{CC} - 2.0V$.
- V_{IHCMR} (Min) varies 1:1 with V_{EE} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

TIMING DIAGRAM



AC ELECTRICAL CHARACTERISTICS(1, 2)

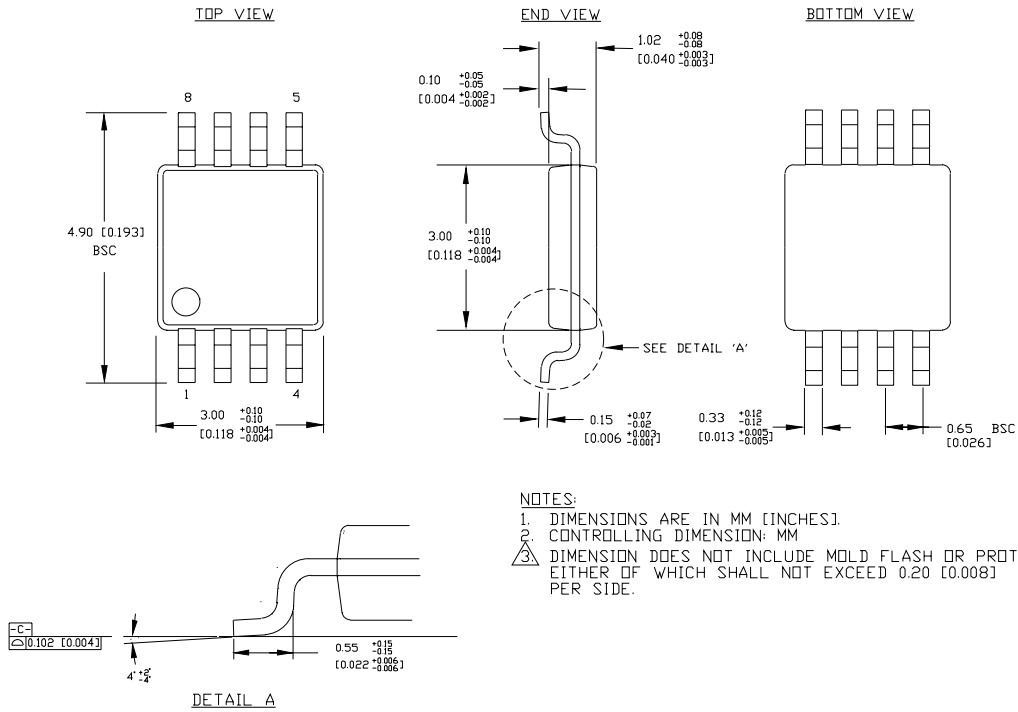
NECL: $V_{CC} = 0V$, $V_{EE} = -3.3V$ to $-5.0V \pm 10\%$; PECL: $V_{EE} = 0V$, $V_{CC} = +3.3V$ to $+5.0V \pm 10\%$.

| Symbol | Parameter | $T_A = -40^\circ C$ | | | $T_A = +25^\circ C$ | | | $T_A = +85^\circ C$ | | | Unit |
|------------------------|---|---------------------|-------------------|-------------------|---------------------|-------------------|-------------------|---------------------|-------------------|-------------------|---------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| f_{MAX} | Maximum Frequency ⁽³⁾ | 4 | — | — | 4 | — | — | 4 | — | — | GHz |
| t_{PLH} t_{PHL} | Propagation Delay to Output CLK → Q (SY10EP33V) RESET → Q (SY100EP33V) RESET → Q | 300 300 310 | 380 420 420 | 440 470 470 | 300 290 310 | 380 420 420 | 440 470 470 | 320 320 320 | 400 450 450 | 460 500 500 | ps |
| t_{RR} | Set/Reset Recovery | 200 | — | — | 200 | 100 | — | 200 | — | — | ps |
| t_{PW} | Minimum Pulse Width RESET | 550 | — | — | 550 | 200 | — | 550 | — | — | ps |
| t_{JITTER} | Cycle-to-Cycle RMS Jitter ⁽³⁾ | — | 0.2 | < 1 | — | 0.2 | < 1 | — | 0.2 | < 1 | ps(rms) |
| V_{PP} | Input Voltage Swing (Differential) | 150 | 800 | 1200 | 150 | 800 | 1200 | 150 | 800 | 1200 | mV |
| t_r t_f | Output Rise/Fall Times Q, /Q (20% to 80%) | 90 | 170 | 200 | 100 | 180 | 220 | 120 | 200 | 240 | ps |

Notes:

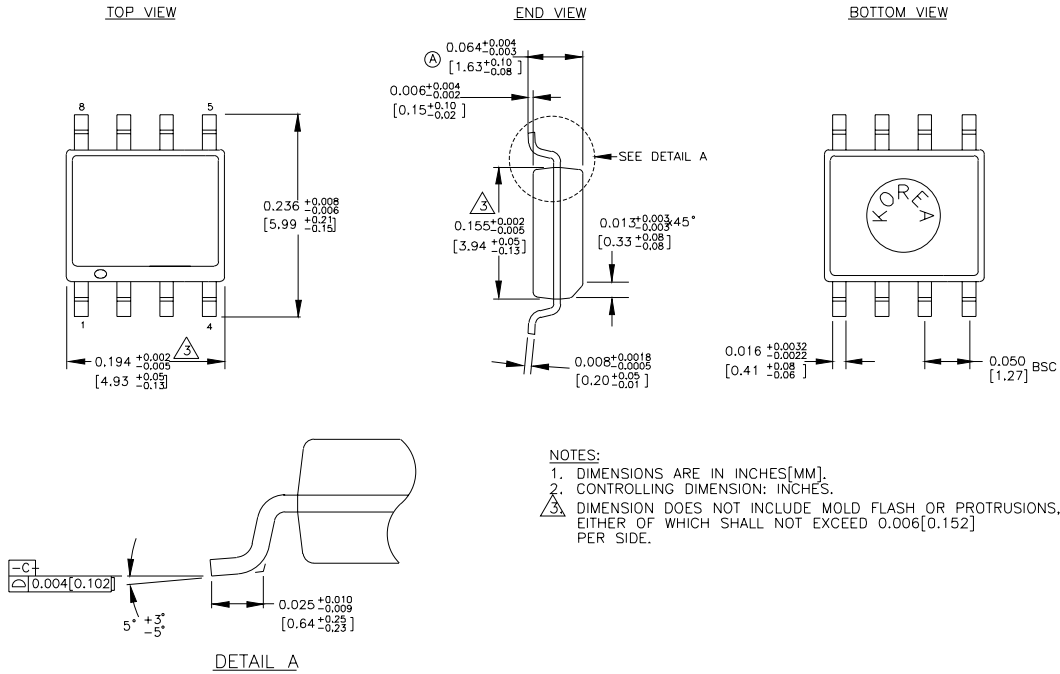
1. Measured using a 750mV source, 50% duty cycle clock source. All loading with 50Ω to $V_{CC} - 2.0V$.
2. Specifications for packaged product only.
3. f_{MAX} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.

8 LEAD MSOP (K8-1)



Rev. 01

8 LEAD SOIC .150" WIDE (Z8-1)



Rev. 03

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